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10/596,422	06/13/2006	Youri Ponomarev	NL031497	6431

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EXAMINER	
WHALEN, DANIEL B	

ART UNIT	PAPER NUMBER
4176	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/596,422	PONOMAREV, YOURI	
	Examiner	Art Unit	
	Daniel Whalen	4176	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 June 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/596,422. Currently, claims 1-10 are pending.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

Figure 3 from drawing does not show reference sign "**IB**" that was described in the specification page 5, line 11. Appropriate correction is required.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of

any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the Claim1, preamble line 1-2 reciting, "forming a strained Si layer on a substrate (1)" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. **Claim 1** is objected to because of the following informalities: Claim 1 is showing antecedent basis issues.

Line 4 "a monocrystalline Si surface" should be changed to -- a monocrystalline Si surface layer --

Line 11 "a monocrystalline Si surface layer" should be changed to -- said monocrystalline Si surface layer --

Claim 7 is objected to because of the following informalities: Instant claim 7, which is depended on claim 1, recites, "said solid phase epitaxy (SPE)" and claim 1 does not recite a solid phase epitaxy. It appeared that claim 1 should be corrected by changing "said strained Si layer by epitaxial growth" to -- said strained Sil layer by a solid phase epitaxy (SPE) -- in order to correct antecedent basis issue.

Claim 1-10 are objected to because of the following informalities: claim 1 recites, "said amorphous Si layer (3B) being adjacent to said buried silicon dioxide layer" should be changed to -- said amorphous Si layer (3B) is on said buried silicon dioxide layer --

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. **Claim 1-10** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Line 2 "a substrate (1)" and line 9-10 "said substrate (1)" and "a support layer (1)" from claim 1 are unclear since both "a substrate" and "a support layer" have the same numerical annotation, (1). It appears from claim 1 is that a numerical annotation (1) from the substrate should be removed since the substrate is a silicon-on-insulator substrate that comprises a support layer, a BOX layer, and a monocrystalline Si surface layer.

Claim1, preamble line 1-2 recites, "forming a strained Si layer on a substrate (1)" is unclear since the substrate is a silicon-on-insulator substrate as it is mentioned on line 9 of the claim 1 and the instant drawing (fig. 7-9) does not show "a stained Si layer on a silicon-on-insulator substrate." Rather, it appears from the drawing that the strained Si layer is either formed on a support layer (1) from fig. 8-9 or a second substrate (10) from fig. 7.

Claim 1, line 6-7 of the instant application recites, "said Si layer" is unclear as to what Si layer is being referred to between a strained Si layer and a monocrystalline Si surface.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. **Claim 1, 4-6, and 8-10** are rejected under 35 U.S.C. 102(e) as being anticipated by Cohen et al. (U.S. 6,774,015 B1; hereinafter "Cohen").

Regarding Claim 1, Cohen teaches a method for forming a strained Si layer on a substrate, comprising:

formation of an epitaxial SiGe layer (item 110) on a monocrystalline Si surface (item 100; col. 4, line 26-52),

formation of said strained Si layer by epitaxial growth of said Si layer on top of said epitaxial SiGe layer, said Si layer having a strained state due to said epitaxial growth, characterized in that (fig. 6; col. 5, line 47-56)

said substrate is a Silicon-On-Insulator substrate comprising a support layer (item 160), a buried silicon dioxide layer (item 150) and a monocrystalline Si surface layer (item 100), said method further comprising (col. 4, line 26-32):

ion implantation of said Si surface layer and said epitaxial SiGe layer to transform said Si surface layer into an amorphous Si layer (item 100') and a portion of said epitaxial SiGe layer into an amorphous SiGe layer (item 110'), a further portion

of said epitaxial SiGe layer being a remaining monocrystalline SiGe layer (*see* fig. 3 and 4; col. 5, line 8-31),

said amorphous Si layer, said amorphous SiGe layer and said remaining monocrystalline SiGe layer forming a layer stack on said buried silicon dioxide layer, with said amorphous Si layer being adjacent to said buried silicon dioxide layer (see fig. 4).

Regarding Claim 4, Cohen teaches method further comprises:

re-crystallizing of said amorphous Si layer and said amorphous SiGe layer by a solid phase epitaxy (SPE) regrowth process at an interface between said remaining monocrystalline SiGe layer and said amorphous SiGe layer (col. 5, line 32-46),

said amorphous Si layer being transformed into an epitaxial strained Si layer and said amorphous SiGe layer being transformed into a re-grown crystalline SiGe layer (col. 5, line 32-46).

Regarding Claim 5, Cohen teaches the removal of said re-grown crystalline SiGe layer by etching (col. 5, line 56-61).

Regarding Claim 6, Cohen teaches that the strained Si layer is a gate channel in a MOSFET structure (col. 1, line 14-45).

Regarding Claim 8, Cohen teaches that the Si surface layer has a thickness of less than 10 nm (col. 4, line 37-43).

Regarding Claim 9, Cohen teaches MOSFET structure comprising source, drain and gate, wherein said gate comprises a gate channel consisting of a strained Si layer;

said strained Si layer being manufactured by a method in accordance with claim 1 (col. 1, line 14-45).

Regarding Claim 10, Cohen teaches semiconductor device comprising at least one MOSFET structure in accordance with claim 1 (col. 1, line 14-45).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. **Claim 2** is rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen as applied to claim 1 above, and further in view of Xiang et al. (US Pub 2004/0087114 A1; hereinafter "Xiang"). Teaching of Cohen has been discussed above. However, Cohen is silent as to patterning the layer stack for forming active parts of a MOSFET. Xiang discloses patterning the layer stack for forming active parts of a MOSFET structure (see fig. 2a, 2b, and 2h; page 3, paragraph 26). Therefore, it would have been obvious to one of the ordinary skill in the art at the time of the invention to integrate the method of Cohen with patterning the layer stack as disclosed by Xiang so as to isolate the region to function as active region that comprises channel, source, and drain.

11. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen as applied to claim 1 above, and further in view of Yu et al. (US 6,410,371 B1; hereinafter "Yu") and Fonstad, Jr. et al. (US 6,455,398 B1; hereinafter "Fonstad, Jr."). Teaching of Cohen has been discussed above. However, he does not teach method of deposition of a silicon dioxide capping layer on said remaining monocrystalline SiGe layer; bonding of said substrate to a second substrate, said second substrate having a silicon dioxide surface layer, said silicon dioxide capping layer on said substrate being face-to-face with said silicon dioxide surface layer; removing said support layer by etching. Yu discloses the followings:

a method of deposition of a silicon dioxide capping layer on said remaining monocrystalline SiGe layer (see fig. 3D; col. 1, line 41-62; col. 3, line 64-67);

bonding of said substrate to a second substrate, said second substrate having a silicon dioxide surface layer, said silicon dioxide capping layer on said substrate being face-to-face with said silicon dioxide surface layer (see fig. 3E; col. 4, line 19-28);

removing said support layer by etching (see fig. 3F; col. 4, line).

Therefore, it would been obvious to one of the ordinary skill in the art at the time of the invention to integrate the method of Cohen with further method discussed above as taught by Yu so as to ensure that the mobility of the carriers is increased.

However, teaching of Cohen as modified by Yu does not disclose removing the buried silicon dioxide layer by etching although buried silicon dioxide layer has discussed (col. 4, line 26-32). Fonstad Jr. teaches removing the buried silicon dioxide

layer by etching (see fig. 1B and 1C; col. 7, line 56 – col. 8, line 17). Therefore, it would have been obvious to one of the ordinary skill in the art at the time of the invention to integrated the method of Cohen as modified by Yu with removing buried silicon dioxide layer by etching as taught by Fonstad Jr. so as to ensure that buried silicon dioxide layer, which functioned as an etch stop layer to prevent damage of device while thinning the substrate, is removed to expose silicon layer for further processing.

12. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen as applied to claim 1 above, and further in view of Yu et al. (US 6,689,671 B1; hereinafter "Yu"). Teaching of Cohen has been discussed above. Also, Cohen teaches solid phase epitaxy for re-crystalization growth by anneal process (col. 5, line 32-46). However, Cohen does not disclose the temperature of anneal process is substantially below 600 °C. Yu teaches low temperature anneal process for solid phase epitaxy from about 500 to 600 °C (col.2, line 5-13; col. 3, line 7-15; col. 6, line 18-25). Therefore, it would have been obvious to one of the ordinary skill in the art at the time of the invention to integrate the method of Cohen with annealing temperature from about 500 to 600 °C so as to minimize deleterious stress relaxation during device processing at high temperature.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rim (US Pub. 2002/0140031 A1)

Christiansen et al. (US Pub 2003/0218189 A1)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel Whalen whose telephone number is 517-270-3418. The examiner can normally be reached on Monday-Friday, 7:30am to 5:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kimberly Nguyen can be reached on (571) 272-2402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Daniel Whalen

Kiesha L. Rose
Primary Examiner
23 Oct. 2007